



1 / 5

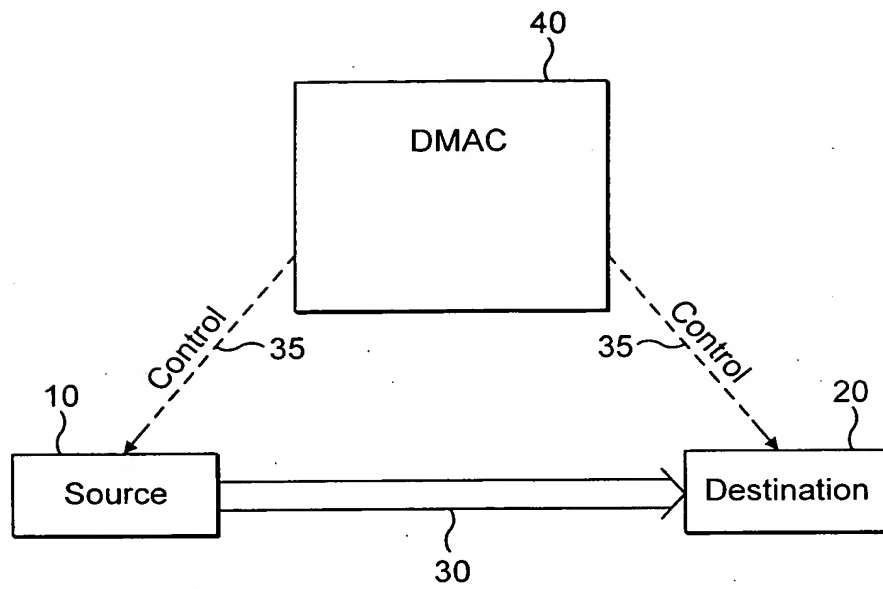


FIG. 1
PRIOR ART

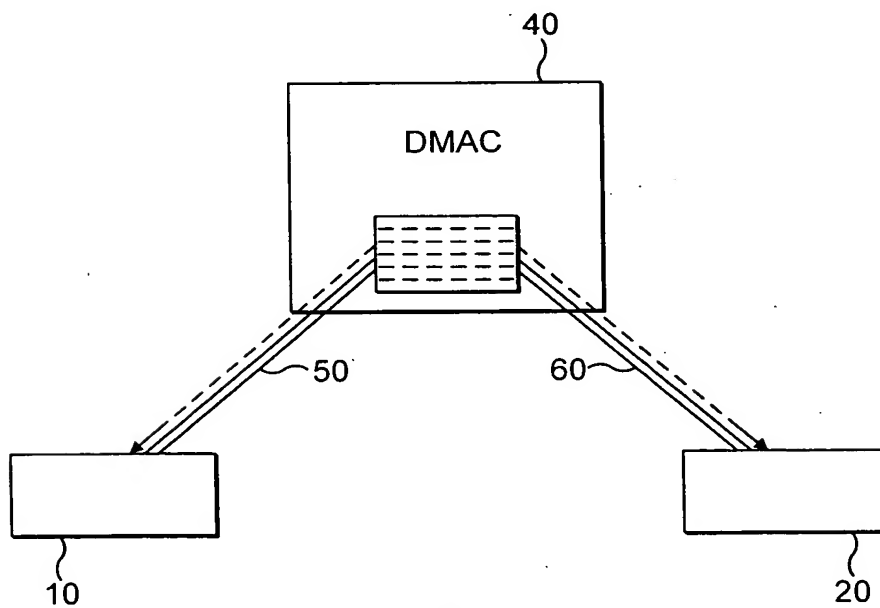


FIG. 2
PRIOR ART

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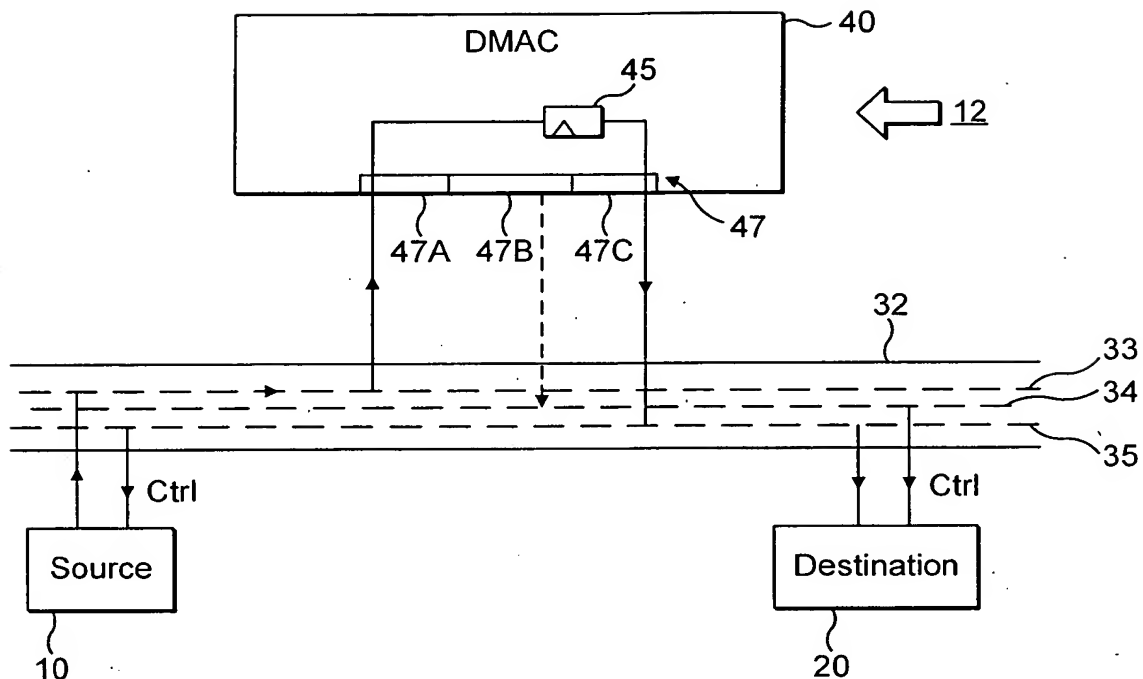
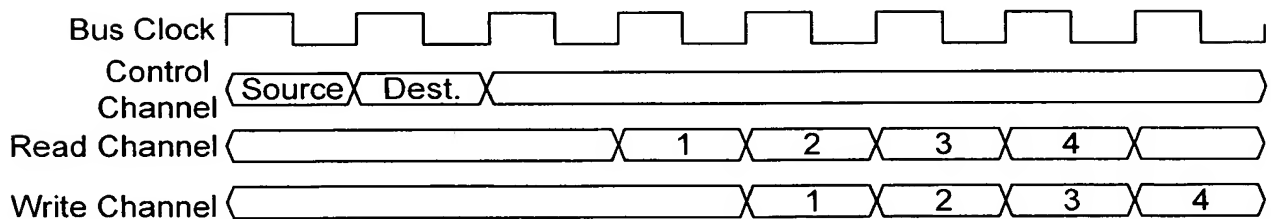


FIG. 3



Example showing 1-cycle delay through DMAC

The DMAC issues the control sequence for the source burst ("Source"), then at some later point issues the control sequence for the destination burst ("Dest") - these are shown in adjacent cycles in this example.

The source services the source burst by placing data items on the read channel. These are delayed by one cycle before being placed onto the write channel by the DMAC.

FIG. 4

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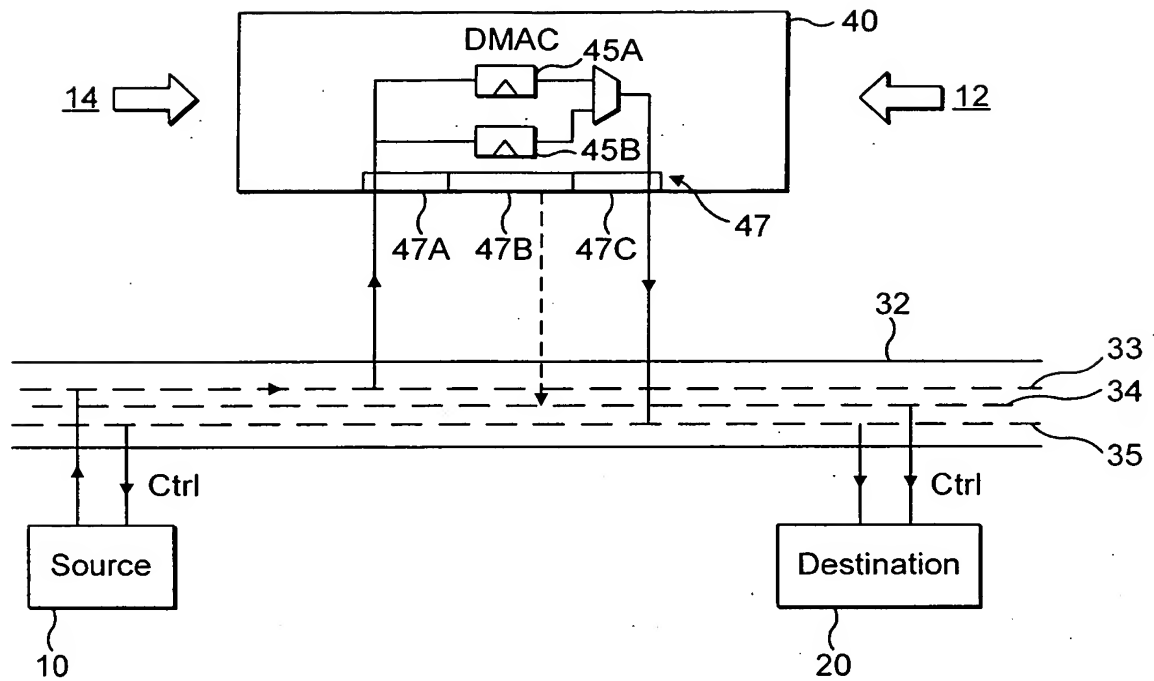


FIG. 5

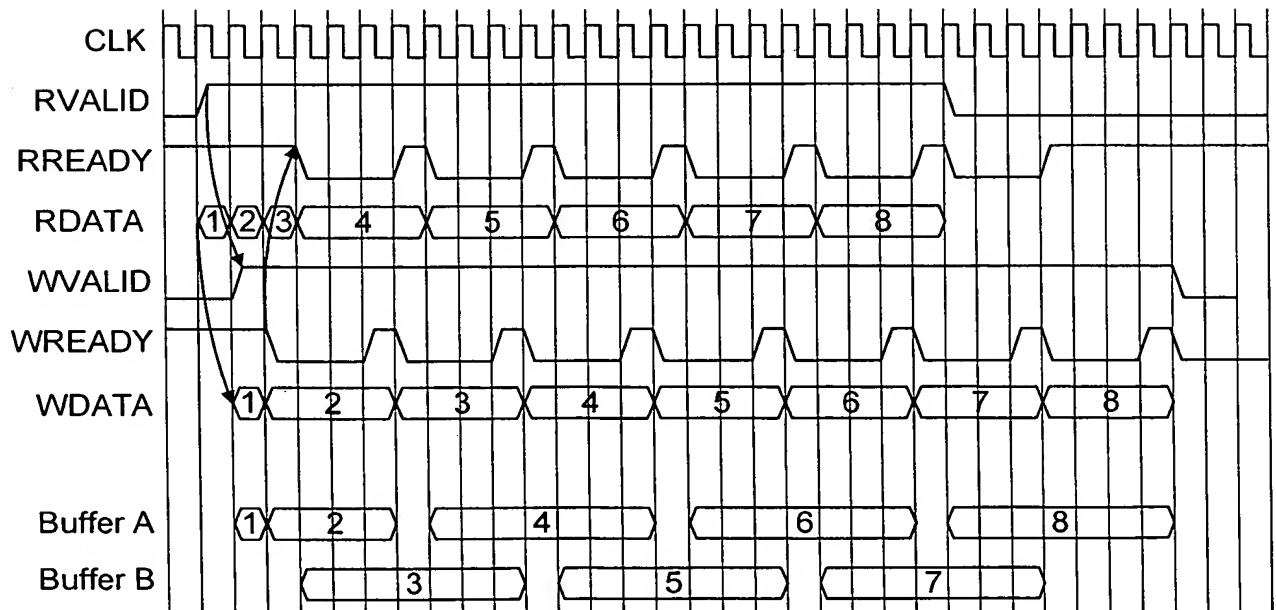


FIG. 6

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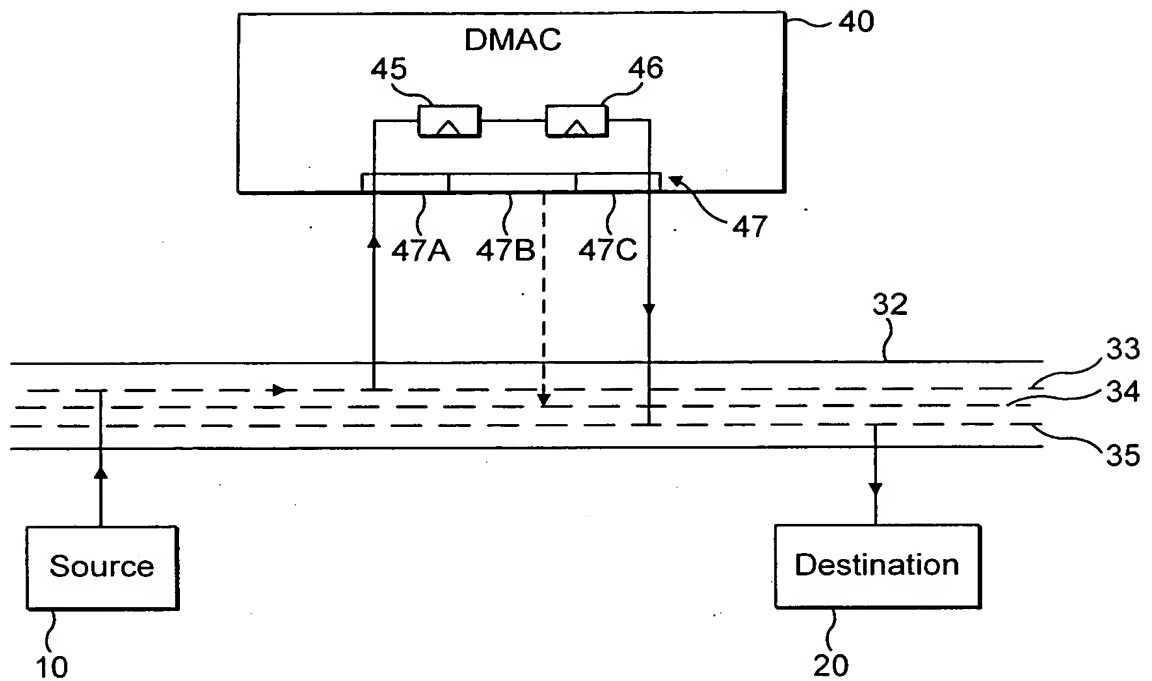


FIG. 7

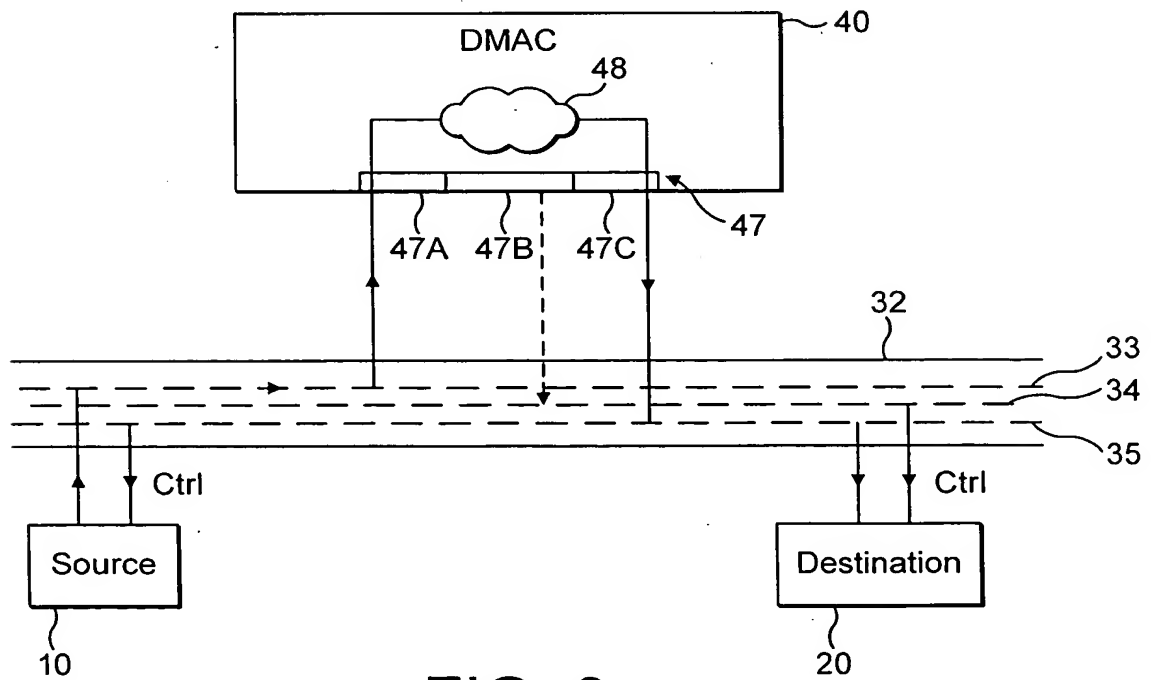


FIG. 8

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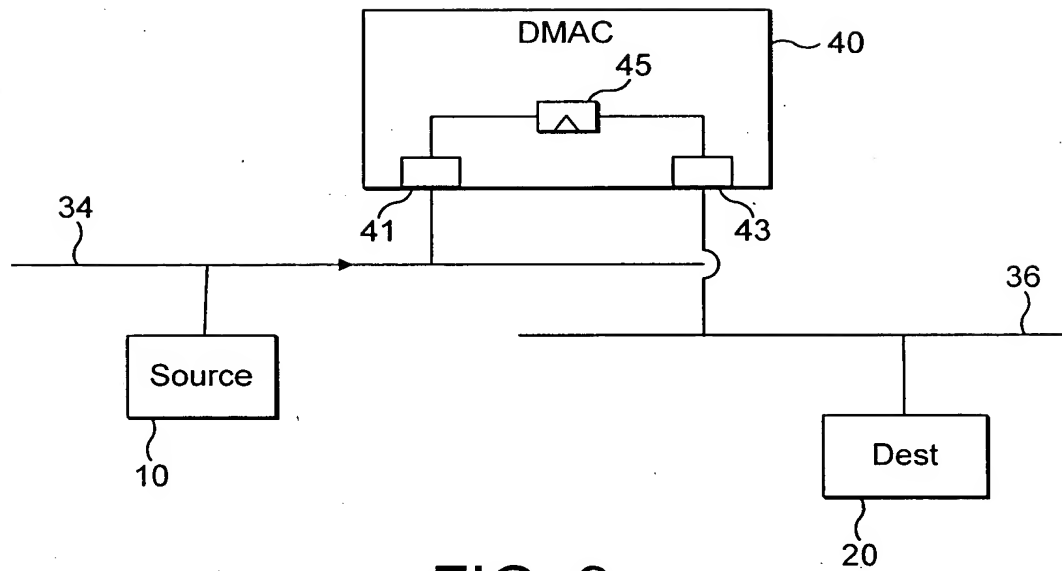


FIG. 9